180nm Low Power CMOS Voltage Comparator

Suraj B. Gawhare
Department of E&TC, D. Y. Patil College of Engineering, Pune, India.

Arati Gaikwad
Department of E&TC, D. Y. Patil College of Engineering, Pune, India.

Abstract – The comparators are main component of many analog to digital converters. The CMOS comparators are widely used in the current technology due to its fast operational speed and high accuracy. The fast growing portable devices requires low power and high operational capabilities which need to be improved. Many of comparator uses CMOS technology, greatly scaled up to 12nm technology file. A brief study of conventional dual tail voltage comparator is done and based on that, a low power and area efficient comparator is presented. A new comparator is designed in order to reduce the delay of conventional comparators and reduce the power consumption of the device. The post layout simulation of proposed comparator is carried out in 180nm CMOS technology consumes 69µW at 1.2V supply voltage.

Index Terms– Complimentary Metal Oxide Semiconductor transistor (CMOS); Ultra Deep Submicrometer (UDSM); Analog-to-Digital Converters (ADCs).

1. INTRODUCTION

The comparator is widely used device next to op- amp in the electronics devices. A low voltage, low power comparator has presented with complete delay analysis for low power applications [1]. A low power CMOS comparator is designed for signal processing applications using bipolar CMOS technology [2]. A low power CMOS comparator in 0.25µm technology is designed for Analog-to-Digital Converter using sigma-delta modulation [3]. A 125 MS/s self-latch low-power comparator is designed in 0.35µm CMOS process which is successfully reduce kickback noise and clock feed through [4].

A low-power CMOS voltage comparator with dual mode quaternary latch is designed in order to consumes less power nearly 20µW at 1.8V supply voltage [5]. The low power CMOS comparator is presented for SAR-ADC applications using preamplifier and latch circuit [6]. A low Power 3-bit flash type ADC is designed based on CMOS comparator designs consumes 130µW at 1.6V supply voltage [7]. An 8-bit 50MS/s low-power voltage comparator has designed in 0.18µm CMOS process with input resolution less than 4mV [8]. An evolutionary algorithm based low power CMOS two-stage comparator has presented in 0.35µm technology approach for low voltage and low power applications [9]. A CMOS comparator with low leakage current, low power consumption is designed using SVL technique [10]. A new comparator is designed in order to reduce the delay of conventional comparators and reduce the power consumption of the device. The post layout simulation of proposed comparator is carried out in 180nm CMOS technology consumes 69µW at 1.2V supply voltage.

2. RELATED WORK

The conventional dynamic dual tail voltage comparator is shown in figure below with complete working and explained some important parameter as follows,

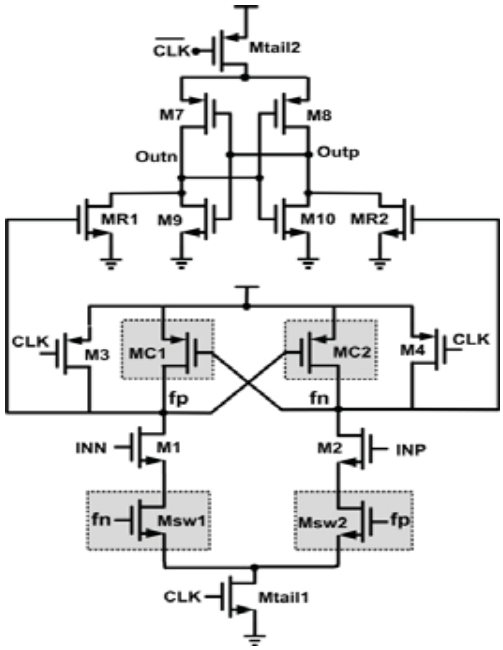

Fig. 1 conventional dynamic dual tail voltage comparator

- Comparator Working
- Power Consumption
- Delay Analysis

2.1. Comparator Working

Fig. 1 shows the conventional dynamic dual tail voltage comparator. The comparator operates in two phases named initial phase and decision making phase. During initial phase

CKL=0, hence the nodes fn and fp are fixed to VDD which makes transistor MR1 and MR2 to conduct (ON). Due to this, both the output nodes are connected to ground.

During decision making phase when CLK=VDD, the charge stored at nodes fn and fp begins to discharge via transistors M1/M2-Msw1/Msw2-Mtail2 to the ground according to the potential applied across the input transistor, suppose voltage across the input INP>INN. The transistor MR2 switched OFF earlier than MR1 and hence the latch generate by the cross coupled inverter which pulls the node Outp to VDD and node Outn remains connected to ground. If INN>INP, the circuit works vice-versa.

2.2. Power Consumption

The cross coupled inverter proposed for latch regeneration is very complex architecture and hence consumes more power for comparison operation. The new latch architecture need to be designed which performs comparison operation with less power.

2.3. Delay Analysis

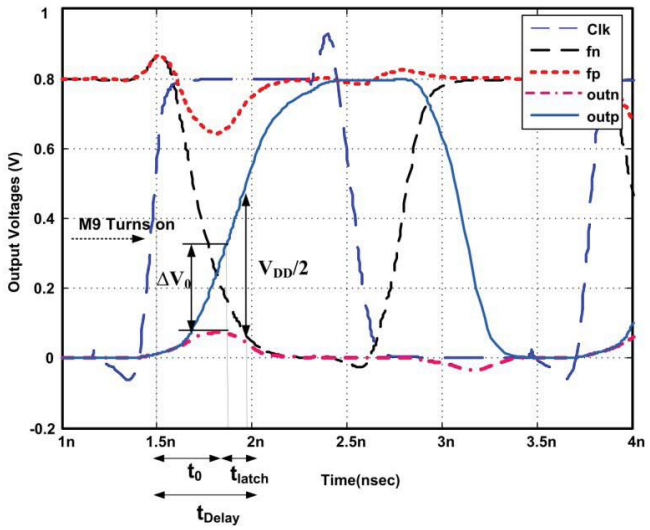

Fig. 2 Transient simulations of the conventional double-tail comparator

Fig. 2 shows the transient simulations of the conventional double-tail comparator. The delay of the comparator is calculated in two parts, latch detection delay (t_0) and latch regeneration delay (t_{latch}). The latch detection delay is the time taken by the comparator to turn OFF one of the transistor MR1/MR2. The latch detection delay is greatly dependents on the transconductance of the M1/M2 transistors. The latch regeneration delay is the time taken by the comparator to generate latch by the cross coupled inverter. The total delay of the comparator is given as, [1]

$$t_{total} = t_0 + t_{latch} \quad (1)$$

The transistors Msw1 and Msw2 are interdependent to the charge potential at nodes fn/fp during decision making phase in order to reduce the power consumption and hence they restrict the flow charge from fn/fp nodes to ground. Due to these, the initial voltage difference of nodes fn and fp reduced which in turn increase the delay of the comparator.

3. PORPOSED COMPARATOR

In order to improve the performance of the dual tail comparator, a new architecture of comparator is proposed by adding few transistors to the conventional dual tail comparator. The complete design of the proposed comparator is shown in the figure below with complete operation and explained the meaningful changes as follows,

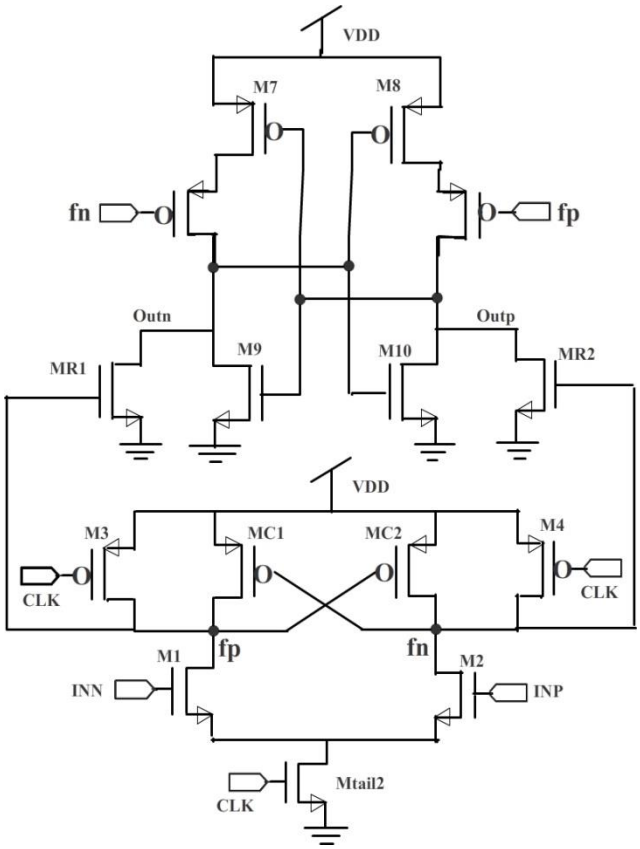

Fig.3 proposed comparator

3.1. Comparator Working

Fig. 3 shows the proposed comparator with the addition of M5 and M6 transistors, gated nodes fn/fp. During initial phase CKL=0, hence the nodes fn and fp are fixed to VDD which makes transistor MR1 and MR2 to conduct (ON). Due to this, both the output nodes are connected to ground. At the same time, the pMOS transistors M5 and M6 are switched OFF to reduce static power loss in the circuit.

During decision making phase when CLK=VDD, the charge stored at nodes fn and fp begins to discharge via transistors M1/M2-Mtail2 to the ground according to the potential applied across the input transistor, suppose voltage across the input INP>INN. The transistor MR2 switched OFF earlier than MR1 and hence the latch generate by the cross coupled inverter which pulls the node Outp to VDD and node Outn remains connected to ground. If INN>INP, the circuit works vice-versa.

3.2. Power Consumption

Fig. 3 shows the proposed comparator with the addition of M5 and M6 transistors, gated nodes fn/fp. During initial phase, the transistors M5/M6 save static power loss by providing strong isolation between VDD to GND. During decision making phase, unless one of the transistor form MR1/MR2 turns OFF, transistors M5/M6 restricts the flow charge from VDD to GND in order to reduce power consumption of the circuit. Hence the overall power consumption of the comparator is reduced.

3.3. Delay Analysis

Fig. 3 shows the proposed comparator without Msw1 and Msw2 transistor. In the absence of these two transistors, the charge flow very quickly from VDD to GND and increase the differential voltage difference between nodes fn/fp. Hence the latch regeneration speed of the comparator is increased.

4. RESULTS AND DISCUSSIONS

The proposed comparator has designed and compared with the existing conventional double-tail comparator in order to understand the performance of the proposed design. The simulation accomplished in Mentor graphics version_10.2 by using TSMC 0.18µm technology file. The schematic layout design of proposed comparator circuit has created in the Pyxis schematic.

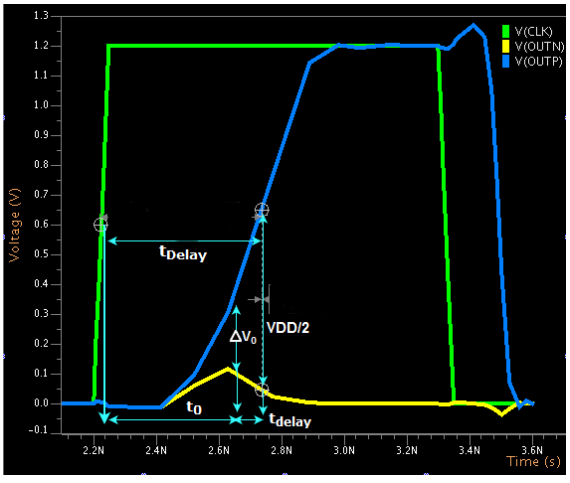

Fig. 2 Transient simulations of the proposed comparator

Fig. 2 shows the transient simulations of the proposed comparator simulated in the Mentor Graphic simulation tool. The latch regeneration delay is reduced by removing transistor Msw1 and Msw2. Both the comparator circuits were simulated in same 180nm CMOS technology at 1.2V supply having same sampling frequency.

Parameters	Double-Tail Comparator	Proposed Comparator
Technology CMOS	180nm	180nm
Supply voltage (V)	1.2	1.2
Sampling freq. (MHz)	450	450
Transistor count	16	15
Power	122 µW	69 µW
t_{latch} (latching delay)	134 ps	81 ps
Total Delay (ps)	392	529
Power Delay Product	47.8×10^{-21} J	36.5×10^{-21} J

Table 1 Comparison of Simulation results of different comparators.

5. CONCLUSION

The complete analysis of the conventional dual tail dynamic comparator is done. Based on that, a new comparator design is proposed which shows better performance than the previous one. The power consumption of new comparator is very low in comparison with the conventional dual tail comparator. The only drawback of the proposed comparator is comes with increase in the latch detection delay due to the addition of M5/M6 transistor. Finally a brief tabular comparison is presented in order to compare the performance of both the comparators. The simulation of both circuits is carried out by Mentor Graphic simulation tool in 180nm CMOS process.

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Author

Suraj B. Gawhare

B.E form OM COE Wardha, at RTM Nagpur University in ENTC.

Currently pursuing M.E from Dr. D Y Patil COE at Pune University in VLSI and Embedded Systems.

Area of interest in research includes VLSI Design.